EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	((hardware adj description adj language) HDL) and asynchronous and (((inter adj process) interprocess) adj communication) and clock and TCP and PLD and embedded and debugger	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L2	16	((hardware adj description adj language) HDL) and asynchronous and (((inter adj process) interprocess) adj communication) and clock and TCP and PLD and embedded and debugger and ((multiple plurality) same software same simulat$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L3	17	((hardware adj description adj language) HDL) and asynchronous and (((inter adj process) interprocess) adj communication) and clock and TCP and debug$3 and ((multiple plurality) same software same simulat$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L4	18	cosimulation and asynchronous	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47

L5	697	simulation and (asynchronous same clock same (maximum threshold reference parameter))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L6	48	simulation.ab. and (asynchronous same clock same (maximum threshold reference parameter))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L7	9	simulation.ab. and (asynchronous same clock same (maximum threshold))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L8	9	simulation.ab. and (asynchronous same delay same (maximum threshold))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L9	0	(cosimulation coverification (co adj simulation)) and (asynchronous same delay same (maximum threshold))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L10	0	(cosimulat$5 coverificat$5 (co adj simulat$5)) and (asynchronous same delay same (maximum threshold))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L11	1	((distributed parallel) adj simulat$5) and (asynchronous same delay same (maximum threshold))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L12	0	((distributed parallel) adj simulat$5) and (asynchronous same clock same (maximum threshold))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47

L13	9	(cosimulation coverification (co adj simulation)) and (asynchronous same clock same (maximum threshold))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L14	240	linearization same simulation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L15	31	linearization same simulation same during	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L16	0	cosimulation.ab. and (asynchronous same (limit threshold))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L17	2	"7218979"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L18	37	timing same violation same percentage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L19	1	timing same erro same percentage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L20	528	timing same error same percentage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47

L21	422	(timing same error same percentage) and circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L22	208	(timing same error same percentage same circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L23	2	(timing same error same percentage same circuit same simulation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L24	33	(timing same error same percentage) and (circuit same simulation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L25	5	(static same timing same error same percentage) and (circuit same simulation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L26	14	(static same timing same error same percentage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L27	32	(boundary adj condition) and stent and load and displacement	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L28	1	asynchronous same readahead	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47

L29	210	asynchronous same clock same cycle same limit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L30	9	(asynchronous same clock same cycle same limit) and (circuit same simulation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L31	200	(asynchronous same clock same cycle same limit) and (circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L32	19	(asynchronous same clock same cycle same limit) and simulation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L33	32	"638379"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L34	2	"6389379".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L35	0	"6389379".pn. and (asynchronous same limit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L36	0	"6389379".pn. and (asynchronous same limit$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47

L37	1	"6389379".pn. and (limit$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L38	2	"5392227" .pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L39	5	(asynchronous same circuit same simulation) and interprocess and HDL	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L40	5	(asynchronous same circuit same simulation) and interprocess and (VHDL HDL Verilog)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L41	374	(asynchronous same circuit same simulation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L42	161	(asynchronous same circuit same simulation) and (HDL VHDL Verilog)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L43	77	"5535342"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L44	2	"5535342".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47

L45	89	PLD same server same image	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L46	53	PLD same server same image same switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L47	10	"7031267"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 13:47
L48	64	(asynchronous same simulation).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 15:17
L49	11	(asynchronous same simulation and (variable dynamic)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 15:17
L50	33	703/14 and l41	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 15:18
L51	23	l50 and (variable dynamic$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 15:18
L52	13	(asynchronous same simulation and (variable dynamic$4)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/15 15:18

| L53 | 22 | l50 and (variable dynamic$4) and (clock period cycle) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/12/15 15:19 |

EAST Search History (Interference)

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